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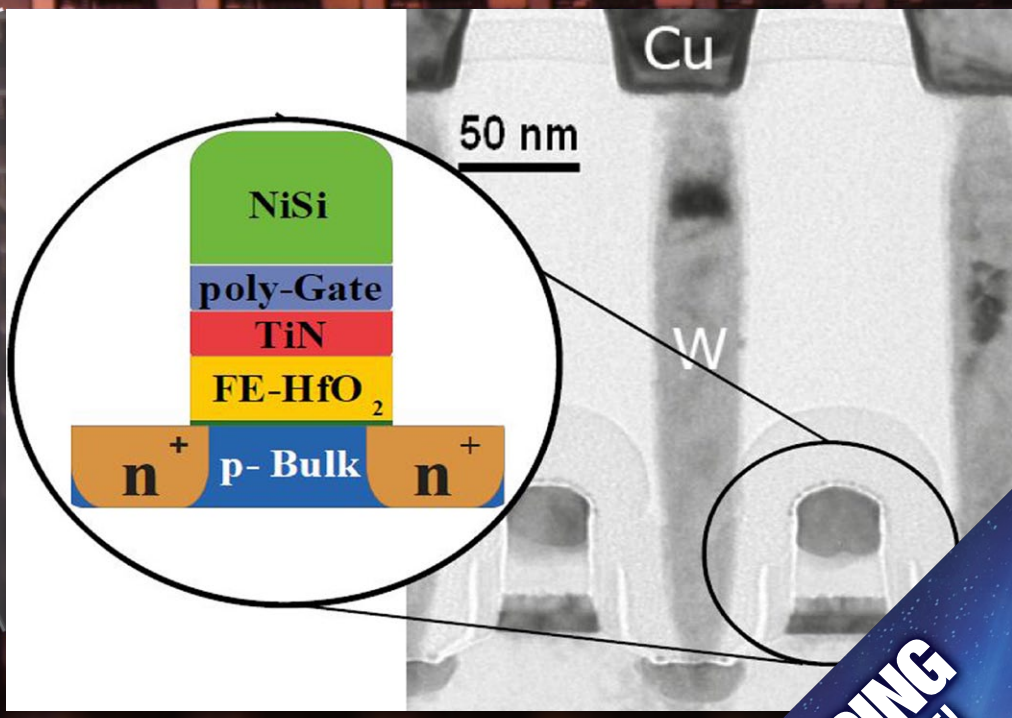
Qimonda's late legacy: 28nm FeRAM



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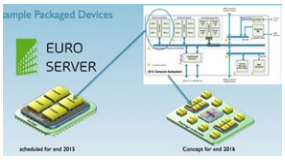

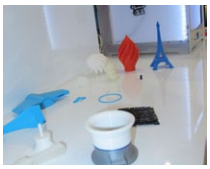

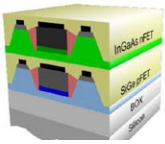

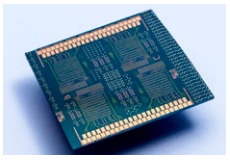

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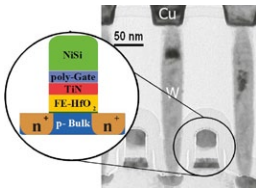
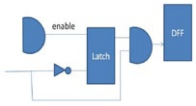
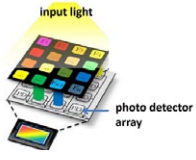






READER OFFER

Qimonda's late legacy: 28nm FeRAM

By Julien happich

CMOS-COMPATIBLE 28NM FERAM could become commercially available within three to five years, according to research from a collaborative project between NaMLab at TU Dresden, the Fraunhofer Institute for Photonic Micro Systems (IPMS) and GlobalFoundries.

Indeed, smashing all prior research claims on FeRAM and scalable to geometries an order of magnitude smaller than today's 130nm FeRAM commercial offerings, the results are so promising that they are being included in the current version of the International Technology Roadmap for Semiconductors (ITRS).

A result of a sub-project called 'Cool Memory' at Saxonys' cluster Cool Silicon, the technology relies on newly found ferroelectric effects in doped Hafnium oxide (HfO_2). Considering that Hafnium oxide is already commonly used as a high-k gate dielectric in CMOS transistors, the processes are pretty much already in place for its ferroelectric variant, readily scalable with CMOS transistors.

So why look at doped Hafnium oxide in the first place?

We asked Dr. Thomas Mikolajiick, Professor for Nanoelectronic Materials and Director of the NaMLab, coordinator for Cool Silicon.

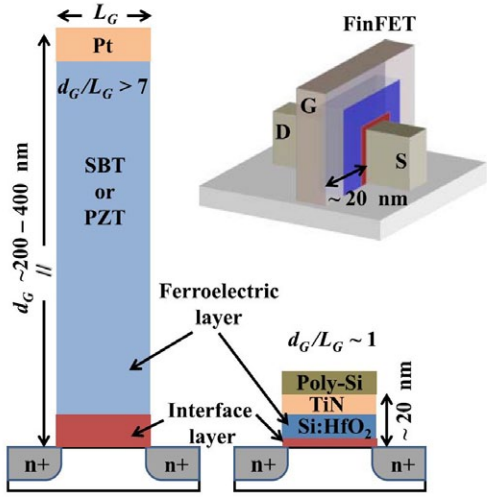
"This research goes back to 2007 at DRAM maker Qimonda, when a PhD candidate Tim Böscke was doing research to improve HfO_2 as a high-k dielectric for capacitors in dynamic random access memories, using dopants to stabilize the material", explained Mikolajiick. "At certain dopant concentrations and under specific treatments, Böscke noticed that strange peaks occurred in the CV characteristic of the material, and that it behaved as a ferroelectric. This was totally unexpected!"

At that time, Qimonda's resources were already shrinking (the company went out of business in 2009), but further investigation was performed at NaMLab, historically created as a joint venture between Qimonda and the University of Technology of Dresden (TU Dresden), to do development work on FeRAM.

Back in 2009, there was still a lot of work to do, notably to make sure that the effects being observed were not just parasitics.

"We've spent the last four to five years characterizing the material's properties and tuning its parameters to make it applicable to FeRAM devices" told us Mikolajiick. "The ferroelectric effects in doped orthorhombic HfO_2 were further corroborated through computational simulation at imec, among other labs".

"The next step was to convince GlobalFoundries to integrate FE-HfO_2 in its CMOS process, and the first samples we have already outperformed all other FeRAM technologies and other non-volatile memories at a comparable node".



Comparing gate-stack structures at the 28nm node – a perovskite-type FeFET, a HfO_2-based FeFET and a FinFET cell design.

So far, FeRAM manufacturers such as TI, Ramtron (recently acquired by Cypress) and Fujitsu are all using lead zirconate titanate (PZT) as the ferroelectric material in one-transistor one-capacitor memory cells. But none of them have been successful in scaling PZT beyond 130nm, because the perovskite-type material is notoriously difficult to deposit and its FE-properties degrade at reduced thickness.

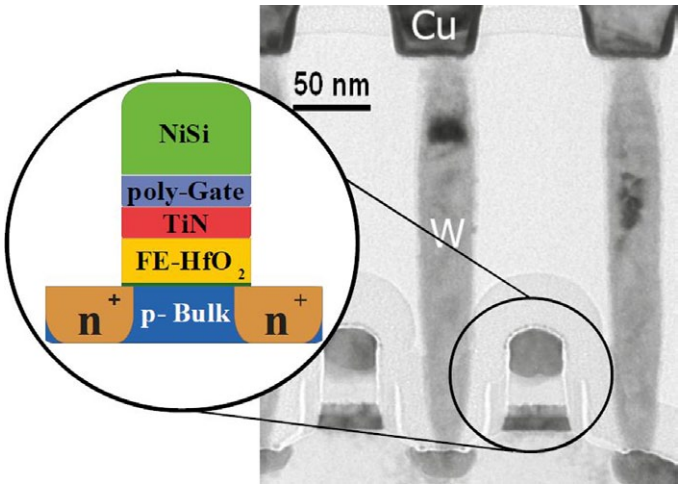
In contrast, the researchers have shown that FE-HfO_2 exhibits stable ferroelectric properties at film thicknesses in the nanometer range (5 to 30nm), which could make ferroelectric field-effect transistors (FeFET) a suitable alternative for non-volatile memory (1T FRAM) in highly integrated 2D or even 3D CMOS designs.

Mikolajiick expects the technology to displace NOR-Flash in embedded memory applications, highlighting that the integration of such FeFETs RAMs is much simpler, requiring only 3 extra steps versus 7 to 10 extra layers for floating-gate based NOR-flash devices.

And again, hafnium oxide is readily available as high-k material in today's CMOS processes, so it is only a matter of adding another gate oxide layer, albeit a ferroelectric one.

In prior research, the NaMLab was also able to demonstrate significantly faster operation speed with program and erase times in the nanosecond range and lower voltage operation.

"Typical technologies currently used for non-volatile memory are based on the principle of charge-storage," Mikolajick says. "This has several disadvantages. Writing, for instance, requires high voltage and is very energy intensive. Due to the high voltage, certain circuit parts for controlling memory cannot be reduced to desired sizes which renders such memory inefficient for small



A micrograph of the Fe-HfO_2 structure.

and medium storage densities."

In comparison, the ferroelectric material in the FeFET can be brought into two different polarization states by means of electric charges, and switching requires very little energy. Data retention measurements performed at 125ºC during a thousand hours proved the longevity of the saturated memory state, the device remaining operational at temperatures as high as 185°C.

Talking about being cost-competitive, the new memory should enable significant cost-savings according to Mikolajiick, since it cuts both on process and material costs and it also scales down nicely beyond any other type of memory so far, without any exotic 3D design intervention. The researcher reckons that such a memory may turn to be half cheaper than competing technologies.

In a first batch produced at the Frauhofer IPMS Center for Nanoelectronic Technologies in collaboration with GlobalFoundries, the researchers have tried various cell arrangements to test different array architectures, mostly variation of NOR-type architectures.

Next on the lab's roadmap is to further reduce the operating voltage, bringing it down as low as possible to reduce the sizing and footprint of peripheral driving circuitry and also to make the devices run faster.

NaMLab acquired the IP before Qimonda went bankrupt and has now applied for patents on FeRAM memory using FE-HfO_2, but Mikolajiick declined to comment on future licensing strategies.

Memory trends: a look ahead

By Janine Love

AS 2014 WAS WINDING down, there was still a lot of talk about 3D memory, mobile memory, high-performance memory, and "next-gen" memory. So what trends and challenges will make the most noise in 2015? EE Times recently spoke with Jennie Grosslight, the memory test product manager at Keysight Technologies, about what she thinks will be the prevailing memory trends in 2015.

As the memory test product manager, Grosslight is responsible for Keysight's logic analysis and compliance test tools for memory applications. With 25 years of experience and an electrical engineering degree from the University of Colorado, she has worked as an R&D engineer, technical marketing engineer, and product marketing engineer. She has been focused on helping engineers analyze and validate memory systems for the past 11 years.

What can we expect for memory in 2015? What are the trends you see?

Price, power, and performance will continue to be the driving features of memory deployment. Both DDR4 and LPDDR4 offer impressive performance improvements and power savings. DDR4 will see broader deployment to replace DDR3 in servers and begin "trickle-down" deployment in high-end desktop workstations. This will improve cloud performance and save power. LPDDR4-based products will hit the market, and mobile memory will take over as the technology driver for the memory industry overall. As DDR4 and LPDDR4 DRAM sales increase, prices will decrease, driving even more design starts with these technologies. Finally, universal flash storage-based products will be formally introduced, laying the foundation for a quantum jump in mobile systems performance and price/performance.

If you could tell engineers one thing about memory test, what would it be?

DDR memory is at the heart of today's cloud computing servers - most of them having at least 24 DIMMs across four channels. With some data centres reporting that DDR memory is the second-highest failure they experience, the need for robust testing of designs continues to grow. To increase margin and overall performance and create a reliable and robust system, close attention to physical layer and functional testing, characterization, and debug to validate that the system is operating within JEDEC specifications is a critical step.

What has surprised you most about memory development over the past 3-5 years?

In the industry, the biggest surprise has been the emergence of the "Memory Wall" as a fundamental issue, its impact on computing architectures, and the incredible burst of innovation it has stimulated. For the past 10 years, memory has progressed along an evolutionary path, with DDR succeeding SDR, then DDR2, DDR3, and DDR4. Now, everything from 3D silicon cubes to distributed memory architectures and completely new signalling methods are in development with some already deployed. Every few months a new possibility seems to emerge for consideration. It's the most interesting time to be involved in memory in the last 20 years. Along this evolutionary path, lower power and increased data rates in LPDDR technologies for mobile applications continues to push the limits. The LPDDR specification in mobile applications now has the performance of DDR technologies in computing.

From a memory test perspective, it is surprising to see that there are servers being shipped without testing to specifications. Simply designing to recommended guidelines and running software tests to validate system operation doesn't validate that the system is operating within specifications. When systems violate functional or parametric specifications for DDR/LPDDR memory, the system may not fail with each violation. However, as the number of violations increase, so does the rate of memory failures. The degree of difficulty in testing different DDR or LPDDR memory is highly dependent on the layout of the system under test and associated subsystem verification. To ensure this verification has occurred, data centres should consider requiring qualification reports.

What are the major stoppers/technical hurdles for mobile memory? Storage?

Reducing power consumption, total memory channel throughput, and signal density are the key requirements and hurdles. Interfaces need to get faster, wider, denser, or some combination of these to improve channel throughput. Packages need to pack more signals, and this increased signal density causes cross-talk effects. Traditional single-ended signalling beyond 3Gbit/s is very hard and power hungry. Very wide I/O using 3D silicon