MEDIA INFORMATION

‘Cool Silicon’ sets International Standards:
Saxon Scientists develop Manufacturing Technology for Non-Volatile Memory Chips

Research from Saxony opens New Possibilities for Semiconductor Industry

DRESDEN, GERMANY, December, 18, 2014. Research results from a collaborative project between NaMLab (TU Dresden), the Fraunhofer Institute for Photonic Micro Systems (IPMS) and GLOBALFOUNDRIES are being included in the current version of ‘The International Technology Roadmap for Semiconductors’, the technical guide for the semiconductor branch. The development project was achieved at ‘Cool Memory’, a sub-project of Cool Silicon, the leading edge cluster for energy efficient micro-and-nanoelectronics funded by the Federal Ministry for Education and Research.

Based on doped Hafniumoxide, the team has developed a cost-effective, energy-efficient ferroelectric non-volatile memory chip that requires low write voltage, can be produced at small structural width and whose production can easily be integrated in common semiconductor manufacturing processes.

Dr. Thomas Mikolajiick, Professor for Nanoelectronic Materials and Director of the NaMLab at TU Dresden, as well as the coordinator for Cool Silicon says the project’s inclusion in the International Technology Roadmap is a confirmation of the success of the team’s innovative work.

“For an innovation made in Dresden to become part of the International Technology Roadmap guidelines, is certainly not commonplace,” Dr. Mikolajiick says. “We are very proud of this accomplishment because the roadmap is followed closely by members of the international semiconductor industry.”

Cool Silicon Project for Non-Volatile Memory Chips

The new technology is a result of the Cool Silicon sub-project called ‘Cool Memory’, developed by participating partners searching for innovative ways to manufacture non-volatile memory.

“Typical technologies currently used for non-volatile memory are based on the principle of charge-storage,” Mikolajick says. “This has several disadvantages. Writing, for instance, requires high voltage and is very energy intensive. Due to the high voltage, certain circuit parts for controlling memory cannot be reduced to desired sizes, which renders such memory inefficient for small and medium storage densities.”

Therefore, the Dresden scientists rely on a different technology. They store data in ferroelectrics, a material that can be brought into two different polarization states by means of electric charge and switching requires very little energy.

“This is nothing fundamentally new,” Mikolajick says. “The approach has been used since the 1950s. Up until now, the problem has been that manufacturing required complicated materials like lead zirconium titanate (PZT). For chip manufacture, this has posed two challenges: manufacturing requires measures that are very intrusive to typical semiconductor processes; and scaling below 120 nanometers is impossible.”

New Material Makes Efficient Memory Chip Manufacturing Possible
In order to realize the dream of a scalable and cost-effective ferroelectric memory chip, Cool Memory relies on hafnium oxide, a material which is already standard in the 28-nanometer production in the factories of project partner GLOBALFOUNDRIES where it is used as a high-k-material (high-k-dielectric). Using doping, the Dresden scientists were able to turn hafnium oxide ferroelectric and they achieved it using conventional manufacturing processes.

Now, the Saxon Leading Edge Cluster is able to produce non-volatile memory chips that enable more energy efficient writing and require lower voltage than chips currently available. They are also much easier to integrate into CMOS (Complementary Metal-Oxide-Semiconductor) processes than conventional ferroelectrics. (CMOS is a technology for constructing integrated circuits.)

Doped hafnium oxide makes manufacturing at very small structural width possible.

"The fact that this innovation is being included into the ITRS shows us how large the interest is especially from the industry," Mikolajick says. "We are delighted that the work of the Leading Edge Cluster Cool Silicon has found such great international resonance."
The first functioning samples of this new version of memory storage-cells scaled to a structural width of 28 nanometers - have already been produced at the Frauhofer IPMS Center for Nanoelectronic Technologies in collaboration with GLOBALFOUNDRIES. According to Fraunhofer project manager Johannes Müller, the results are very promising:

"In the near future we hope to be able to equip microchips for future generations of more energy efficient smart phones, for instance, with memory developed and produced in Dresden," Müller says. "This would be a huge success for Dresden scientists and for Dresden as an industry location."

About the International Technology Roadmap for Semiconductors
This world-renowned technical guide is issued by associations from five regions that hold leading market positions in the semiconductor branch: The European Semiconductor Industry Association (ESIA); Japan Electronics and Information Technology Industries Association (JEITA), Korean Semiconductor Industry Association (KSIA), Taiwan Semiconductor Industry Association (TSIA) and the U.S. Semiconductor Industry Association (SIA). The ITRS teams examine current trends in research and technology and search for innovative new products of the future as well as promising materials, processes and new manufacturing technologies. For additional information go to http://public.itrs.net.

About Cool Silicon
Cool Silicon is an annual research project funded by the Federal Ministry for Education and Research as part of the Ministry's leading edge cluster initiative. More than 60 enterprises and research institutes of Silicon Saxony are partners in the project in order to develop technologies that significantly reduce energy consumption of microchips and information technologies.

For more information go to: http://www.cool-silicon.de

Additional information at: http://www.spitzencluster.de

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