BeFerroSynaptic

BEOL TECHNOLOGY PLATFORM BASED ON FERROELECTRIC SYNAPTIC DEVICES FOR ADVANCED NEUROMORPHIC PROCESSORS

Project Overview

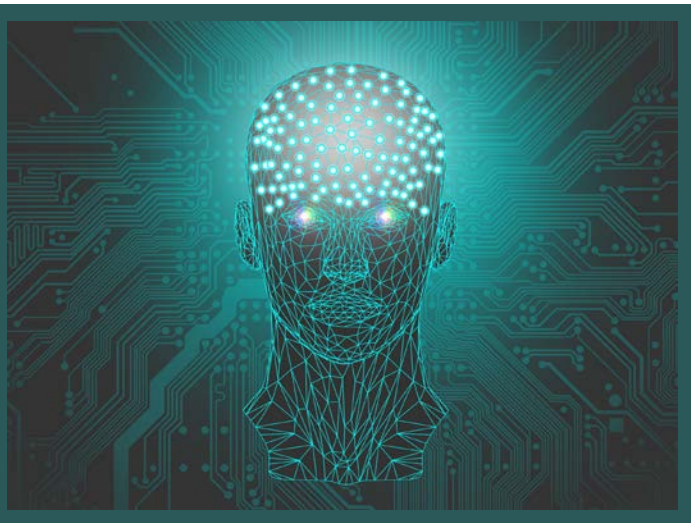
Funded under: H2020-EU.2.1.1.

Overall budget: € 3.998.928,75

Duration: 1 January 2020 - 31 December 2022

Coordinated by: NaMLab gGmbH, Germany

BeFerroSynaptic is funded by the European Union's Horizon 2020 research and innovation programme under Grant Agreement No 871737).
This document reflects only the author's view and the EU is not responsible for any use that may be made of the information it contains.



The increasing amount of data that has to be processed in today's electronic devices requires a transition from the conventional compute centric paradigm to a more data centric paradigm. To bridge the existing gap between memory and logic units that is known as the classical von Neumann bottleneck the concept of physical separation between computing and memory unit has to be repealed. Neuro inspired architectures constitute a promising solution where both logic and memory functionality become synergized together in one synaptic unit.

The ultimate goal of BeFerroSynaptic is to develop a technology platform based on back-end-of-line (BEOL) integrated ferroelectric HfO2-based synaptic devices to tackle the challenges of next generation electronic devices. Our attempt is **to demonstrate the feasibility** of its adoption in an extremely energy-efficient neuromorphic computing architecture that goes far beyond the conventional CMOS paradigm.

The projects' ambitious goal is **to overcome the well-known von Neumann bottleneck**'s data transfer restriction and to bridge the gap between memory and logic units, can be achieved by locating the memory units next to the computation engines. This approach takes its cue from neuro inspired architectures, where both logic and memory functionalities become synergized together in one synaptic unit.

Energy efficiency is key and can be achieved through an extremely low power consumption, mainly via four concepts:

1. The combination of memory and computing functionalities within one single unit.
2. Asynchronous functioning of SNN chips instead of "always ON-clock frequency synchronization" of conventional CPU/GPU.
3. Utilization of single analogue switching mechanism in densely connected convolutional neural networks (CNN).
4. Adoption of time dependent information processing, similarly to what happens in spiking neural networks, where any event generates feedback connections between different layers of the neural network at an inherently low power.

IN THIS ISSUE

CONSORTIUM

The BeFerroSynaptic consortium is formed by 11 partners coming from 5 different countries (Germany, France, Switzerland, Italy, Greece):

- NaMLaB gGmbH (Germany)
- Technische Universität Dresden (Germany)
- X-FAB Dresden GmbH & Co. KG (Germany)
- Commissariat à l'énergie atomique et aux énergies alternatives (France)
- IBM Research GmbH (Switzerland)
- Helmholtz-Zentrum Berlin für Materialien und Energie GmbH (Germany)
- University of Zurich (Switzerland)
- Universitaet Bielefeld (Germany)
- I Consorzio Nazionale Interuniversitario per la Nanoelettronica (IU.NET) with
- Università di Modena e Reggio Emilia (Italy)
- Università di Udine (Italy)
- National Centre of Scientific Research "Demokritos" (Greece)
- Eidgenoessische Technische Hochschule Zuerich (Switzerland)

CONTACT

Coordinator:

Dr. Stefan Slesazeck

NaMLab gGmbH
Dresden, Germany

E-mail:

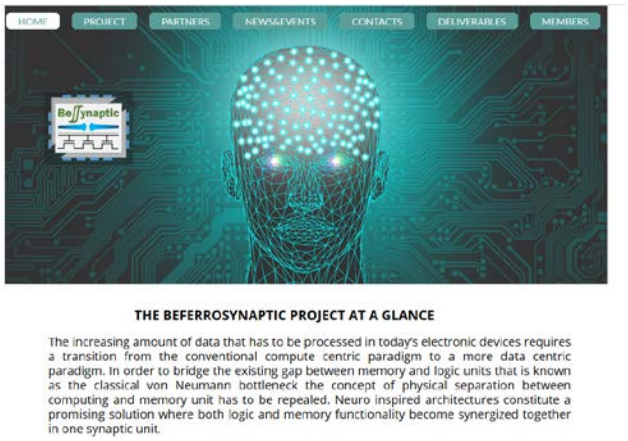
Stefan.Slesazeck@namlab.com

DISSEMINATION ACTIVITIES

Project Website

The website of the BeFerroSynaptic project is online since February 2020. It aims at promoting the project, its activities such as workshops and trainings and competences of our partners

The project URL is: www.BeFerroSynaptic.eu



LinkedIn Group

A joint LinkedIn group has been created to communicate the ongoing activities and disseminate the project results.

The LinkedIn's group name is BeFerroSynaptic and one can join the group via https://www.linkedin.com/groups/8909110/

Instagram

The project uses Instagram as a self-standing repository for all project-related images and pictures available for the public.
https://www.instagram.com/BeFerroSynaptic

Facebook

The project's Facebook group will be mostly used for exchanges among members and interested people from the research community.
https://www.facebook.com/BeFerroSynaptic

Twitter

In order to share short comments, make announcements that can instantaneously reach a large audience or retweet relevant content, the project also has a twitter account set up:
https://twitter.com/BeFerroSynaptic

DELIVERABLES D2.4 AND D3.4

Initial SPICE models for FeFET (D3.4)

To exploit the full potential of neuromorphic circuits containing ferroelectric elements, suitable models to emulate these are vital. The general model describing the ferroelectric polarization switching in a ferroelectric material layer is used for both - implementing the FeFET as well as the FTJ model.

A behavioural model of the ferroelectric layer based on the Preisach model of hysteresis was created to be used in modelling of ferroelectric capacitors (FeCap). To utilize it in SPICE circuit simulations, the implementation was accomplished using Verilog-A. The occurrence of unsaturated sub-loops and a time-dependence of the hysteresis loop as well as the memory wipe-out was introduced in the model (see Fig. 1 a) and 1 b)).

Deliverable D3.4 concerns the provision of an initial FeFET SPICE model for further adaption in Task 3.4 based on electrical characterization results as well as TCAD simulations to fit the devices parameters from Task T3.2 and T3.3 and will be provided to WP5 for circuit design. A series connection of the FeCAP together with a standard transistor model yields the ferroelectric field effect transistors (FeFET) model. As evidenced by the data shown in Fig. 1c) experimental data and simulation results are in good agreement.

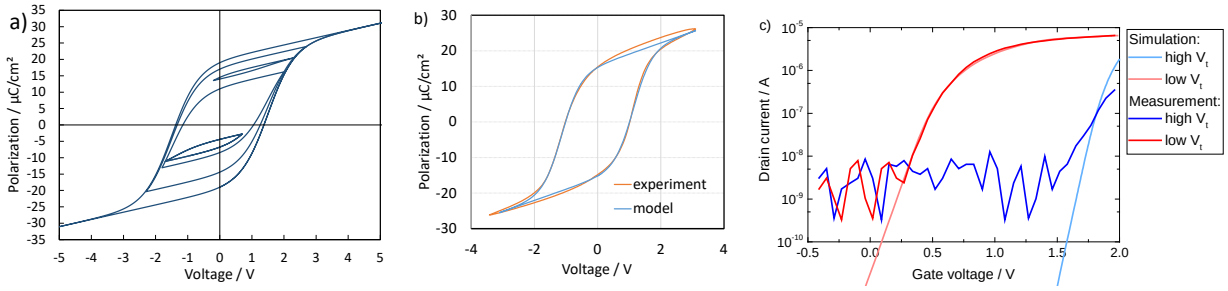


Figure 1: a) Simulated P-E- hysteresis loop of the ferroelectric capacitor, including subloops and memory wipe out. b) Simulated and experimental hysteresis loop a ferroelectric capacitor. c) Simulated and experimental hysteresis loop of a FeFET.

Initial SPICE models for FTJ (D2.4)

Our deliverable D2.4 concerns the provision of an initial FTJ SPICE model for further adaption in Task 2.4 to fit the devices parameters based on electrical characterization results from Tasks T2.1 to T2.3 and will be provided to WP5 for circuit design. Therefore, the ferroelectric switching model of the FeCap was adapted to fit the switching characteristic of the ferroelectric-dielectric bi-layer structure of the composite stack FTJ (see Fig. 2). In contrast to the pure ferroelectric layer this bi-layer exhibits an increased coercive field.

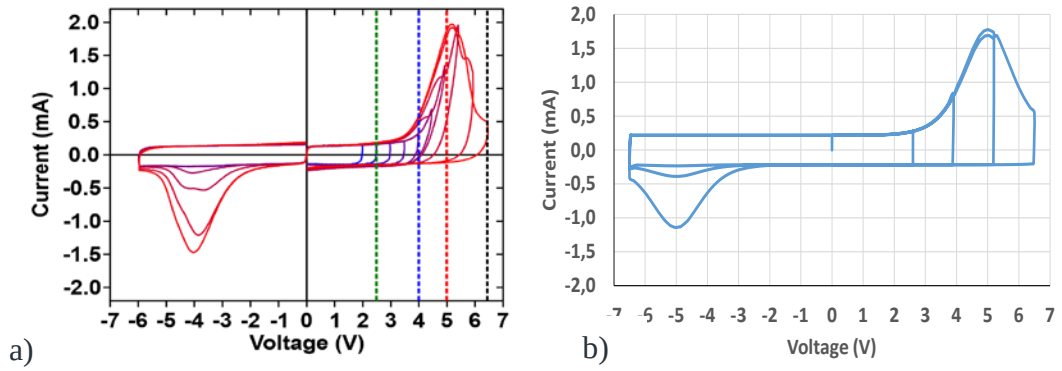


Figure 2: Polarization current of a composite stack FTJ. a) Measured current-voltage response from setting both polarization states, dashed lines indicate the different voltages used for setting the P↑ state for circular FTJ devices with a diameter of 200µm. b) Simulated current-voltage response for the same device based on the Verilog-A model with adapted polarization parameters.

Moreover, in order to model the FTJ static current an additional term that describes the FTJ current phenomenologically was introduced. The comparison of experimental data and simulation results reveals the accuracy of the model (see Fig. 3). In this initial model so far no retention behaviour is included.

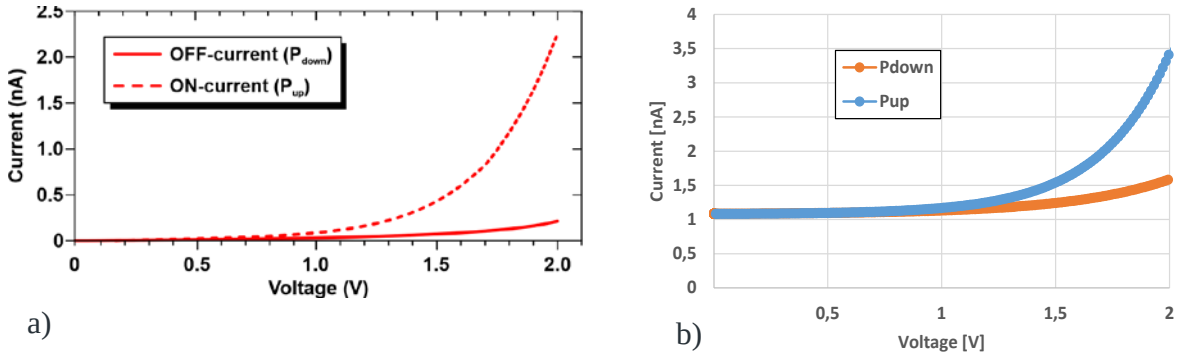


Figure 3 a) simulated FTJ current after setting the FTJ in LRS or HRS by application of voltage pulses of +/- 6.5V. b) measurement results of the device shown in Fig. 1.2-2 using a DC-sweep by a Keithley 4200 SCS and b) simulation results for a continuous voltage ramp with a slew rate of 1.3V/s, adopting the Verilog-A FTJ model as described above.

The SPICE models are provided to the project partners via the project intern share drive. Moreover, the models might be provided to interested researchers upon request. The request should contain a description of the planned use that should be restricted to non-commercial application. Upon publication of results that are based on the application of this model the BeFerroSynaptic project and funding by the European Union's Horizon 2020 research and innovation programme under grant agreement No 871737 should be acknowledged appropriately.

PROJECT MEETINGS

Kick-Off Meeting, January 2020 in @IBM in Zurich, Switzerland

The BeFerroSynaptic Kick-Off Meeting (KOM) took place at @IBM premises in Zurich (Switzerland) January 15, 2020.

The objective of the KOM was to bring together all partners – partly first time they met - and to set up a common team spirit. During the meeting all were made aware of the project's objectives, assumptions, constraints, deliverables, challenges, methodologies, procedures, plans and the working environment.

Kick-off meeting in Zurich, January 2020